Claims

1. A pulse width modulation current adjustment apparatus, comprising:

a triangle wave generator for generating a triangle wave signal;

a comparator;

a field effect transistor;

a power supply;

a first resistor; and

a second resistor;

wherein the triangle wave signal and a modulation signal are input to the comparator, and an output of the comparator is connected to a gate terminal of the FET, the first resistor is connected between the power supply and a source terminal of the FET, and a drain terminal of the FET outputs a driving current through the second resistor to a load.

2. A pulse width modulation current adjustment apparatus as described in claim 1, wherein the triangle wave signal is a symmetric triangle wave signal.

3. A pulse width modulation current adjustment apparatus as described in claim 1, wherein the field effect transistor is an N-channel enhancement-type FET.

4. A pulse width modulation current adjustment apparatus as described in claim 1, wherein the field effect transistor is a P-channel enhancement-type FET.

5. A pulse width modulation current adjustment apparatus as described in claim 1, wherein the field effect transistor is an N-channel depletion-type FET.

6. A pulse width modulation current adjustment apparatus as described in claim 1, wherein the field effect transistor is a P-channel depletion-type FET.

7. A method of making a pulse width modulation current adjustment apparatus, comprising steps of:

providing a triangle wave generator for generating a triangle wave signal;

connecting a comparator to said triangle wave generator;

connecting a voltage source to said comparator;

connecting said comparator to a gate terminal of a filed effect transistor (EFT);

connecting a power supply to a source terminal of via a first resistor; and

connecting a load to a drain terminal of the FET via a second resistor.

8. A triangle wave generator for use with a pulse width modulation current adjustment apparatus, comprising:

a first operational amplifier (15);

a front resistor (23) electrically connecting a negative terminal of the amplifier (15) to ground;

a first feedback resistor (21), a second feedback resistor (22) and a current limiting resistor (24) electrically connecting to a positive terminal of the amplifier (15) so as to form a zero-crossing comparator;

a second operational amplifier (16), a current limiting resistor (18) and a capacitor (17) together forming an integrator;

a back grounding resistor (25) electrically connected a positive terminal of the amplifier (16) to ground; and

an output of the first operational amplifier (15) electrically connected to said positive terminal via said current limiting resistor (24) and said first feedback resistor (21), respectively, and an output of the second operation amplifier (16) electrically connected to the positive terminal of the second operational amplifier (16) and also electrically connected to the positive terminal of the first operational amplifier (15) via the second feedback resistor (22).